

PATENT APPLICATION

**FLIP CHIP IN LEADED MOLDED PACKAGE AND METHOD OF
MANUFACTURE THEREOF**

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**FLIP CHIP IN LEADED MOLDED PACKAGE AND METHOD OF
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BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to an improved package and method of packaging for a flip chip, and more particularly, to a flip chip wherein a die is attached to a leadframe that is then placed within a thinner package such that the back side of the die is exposed.

2. Description Of The Prior Art

In power transistor packages, those in the art are generally still using chip and wire bond interconnect technology. It is difficult to simplify the manufacturing process flow as all process steps, such as, for example, die attach, wire bond, and molding are required. As a result, there is a limit placed on the maximum size for the die. Thus, power transistor packages are suited for single die applications since formation of an isolated metal pad for power transistor packages that include multiple dies is very difficult.

Recent attempts to improve packaging of chip devices have included directly coupling lead frames to the die. However, this technology does not lend itself well to the manufacture of thinner outline (or profile) packages. Hence, such packages, as well as those using wire bond interconnect technology, tend to be thick.

SUMMARY OF THE INVENTION

The present invention provides a chip device that includes a leadframe including a plurality of leads and a die coupled to the leadframe. The die includes a metallized back side as well as source and gate terminals opposite the metallized backside. The die is coupled to the leadframe such that the leads of the leadframe are

directly coupled to the terminals. The chip device also includes a body including a window defined therein. The body is placed around at least a portion of the leadframe and the die such that the metallized back side of the die is adjacent the window.

5 In accordance with one aspect of the present invention, the die is coupled to the leadframe with solder bumps.

In accordance with another aspect of the present invention, the chip device includes two dies.

10 In accordance with a further aspect of the present invention, a method of making a chip device includes providing a leadframe including a plurality of leads and a die attach pad and post, coupling a die to the die attach pad and post and, encapsulating at least a portion of the leadframe and die such that a metallized back side of the die is adjacent a window defined within the package mold.

In accordance with another aspect of the present invention, the method includes configuring leads of the leadframe.

15 In accordance with another aspect of the present invention, the configuring of the leads includes removing mold flashes and resins from the leads, removing dambars, and solder plating the leads.

In accordance with a further aspect of the present invention, the leadframe is provided with preplated leads.

20 In accordance with yet another aspect of the present invention, the leadframe is provided with preplated leads and preformed leads.

In accordance with a further aspect of the present invention, the leadframe is provided with two die attach pads and posts, wherein a first die is coupled to a first die attach pad and post, and a second die is coupled to a second die attach pad and post.

25 In accordance with another aspect of the present invention, the die is coupled to the leadframe die attach pad and post via solder bumps, wherein the solder bumps are re-flowed.

Thus, the present invention provides a chip device that includes a thinner package, yet can accommodate a larger die. Indeed, up to a 70% increase in die area over wire bonded parts may be realized. Additionally, the present invention lends itself to packaging multiple dies in the same package. The present invention allows a die-to-die connection to be achieved using a low resistance path (leadframe based) capable of carrying high current. Furthermore, the present invention provides a simplified

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manufacturing process, especially in the embodiments where preplated and preformed leadframes are provided.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred exemplary
5 embodiments, found hereinbelow, in conjunction with reference to the drawings, in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a top plan view of a chip device in accordance with the
10 present invention;

Figure 1B is a bottom elevation view of a chip device in accordance with the present invention;

Figure 1C is a sectional view of a chip device in accordance with the present invention as seen along the line A-A in Figure 1A;

15 Figure 1D is a side elevation view of a chip device in accordance with the present invention;

Figure 2 is a top plan view of a leadframe for use in making a chip device in accordance with the present invention;

20 Figure 3 is a top plan view of an alternative leadframe for use in making a chip device in accordance with the present invention;

Figure 3A is a top plan view of the leadframe illustrated in Figure 3 a common die attach pad for two dies;

Figure 4 is a top plan view of a die for use in making a chip device in accordance with the present invention;

25 Figure 5 is a bottom plan view of a die coupled to a leadframe and encapsulated with a mold compound;

Figure 6 is a top plan view of a mold compound encapsulating a die coupled to a leadframe with dambars removed and marking on the mold compound;

30 Figure 7A is a top plan view of a preplated and preformed leadframe in accordance for making a chip device in accordance with an alternative embodiment of the present invention; and

Figure 7B is a sectional view of the leadframe illustrated in Figure 7A as seen along the line A-A.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

A chip device or semiconductor device 10 includes a leadframe 11, a chip or die 12 and a mold compound or body 13. Preferably, backside 14 of the die is metallized.

Figure 2 illustrates a leadframe 11a including a plurality of leads 20 and a die attach pad 21a and post 22a. Preferably, the leadframe consists of a copper base and is either silver plated or nickel plated on the die attach pad and post. Figure 3 illustrates a leadframe 11b similar to leadframe 11a. Leadframe 11b includes two die attach pads and posts 22b and thus is used for a chip device that includes two chips or dies. Thus, chip devices with multiple dies may be made. While Figure 3 illustrates two die attach pads, it should be readily apparent to those skilled in the art that leadframes with more than two die attach pads may be used, and hence, chip devices with more than two dies may be made.

Figure 3A illustrates leadframe 11c that includes a common die attach pad 21c for two dies thus providing a die-to-die connection. By using such a leadframe to couple two dies, a low resistance path capable of carrying high current is achieved. For example, in MOSFET devices, this allows bi-directional switches to be fabricated (common source contact).

Figure 4 illustrates a die or chip 12. As noted above, back surface 14 of the die is preferably back metallized. Preferably, top surface 30 of the die is passivated and includes a plurality of solder bumps 31. Most of the solder bumps will serve to connect source region 32 of the chip to leads of the leadframe. Solder bump 33 serves as a gate bump and thus couples gate region 34 of the chip to a gate lead of the leadframe via die attach post 22.

Once the chip with the array of solder bumps is brought into contact with the die attach pad and post, the solder is reflowed, preferably with heat, in order to attach the chip to the leadframe and to provide good contact between the chip and the leadframe.

Once the solder has been reflowed, the chip device is encapsulated with mold compound 13 such that the chip and the die attach pad and post are enveloped by the mold compound.

As can be seen in Figure 5, mold compound 13 includes a window 40 defined therein. The chip device is encapsulated by the mold compound such that

metallized back surface 14 of the die is adjacent to the window. Preferably, as can be seen in Figure 1C, metallized back surface 14 is at least partially within window 40 such that back surface 14 is substantially flush with back surface 41 of mold compound 13.

Thus, after encapsulating the chip device with the mold compound, the metallized back surface of the die is exposed through the window. When the chip device is placed on a circuit board for use, this exposed back surface of the die serves as the drain terminal of the chip device.

Once mold compound 13 has been added to the chip device, the "package" of the chip device is essentially complete. Dambers 50 are removed and the leads are cleansed of any mold flashes and resins that may have accumulated during the manufacturing process. If desired, top surface 51 of the mold compound opposite the surface that includes the window may be marked with a laser or ink as shown in Figure 6, for example, to identify the chip device. The leads are then solder plated and rails 52 at the end of the leads are removed. The leads are then configured by bending or forming them so that the chip may be placed on a circuit board. As can be seen in Figure 1C, the leads are configured so that the ends are essentially co-planar with the exposed back surface 14 of the die.

In accordance with an alternative manufacturing process, the leadframe is pre-plated prior to the start of the manufacturing process. Preferably, the leadframe is pre-plated with NiPd. The manufacturing process proceeds as described above except the step of solder plating the leads is no longer required.

Additionally, in accordance with yet another embodiment of the manufacturing process, the leads of the leadframe are "pre-formed." Preferably, prior to the manufacturing process, the leadframe is plated with NiPd and the leads of the leadframe are pre-formed and configured, as can be seen in Figures 7A and 7B. Thus, the manufacturing process will proceed as outlined above, but the steps of plating the leads with solder and configuring the leads is no longer required.

Accordingly, by providing leadframes for the manufacture of a chip device in accordance with the present invention wherein the leadframes are pre-plated and/or the leads are pre-formed, the manufacturing process may be simplified and shortened. This allows for a quicker, more efficient and less expensive manufacturing process to be realized.

Die 12 may be manufactured in a conventional manner generally known in the art for a number of applications.

Thus, the present invention provides a chip device that includes a thinner package, that can accommodate a larger die by using a single leadframe and using the
5 back metallized surface of the die as drain contacts. Indeed, up to a 70% increase in die area over wire-bonded parts may be realized. Furthermore, the present invention provides a simplified manufacturing process, especially in the embodiments where pre-plated and pre-formed leadframes are provided.

Although the invention has been described with reference to specific
10 exemplary embodiments, it will be appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.